UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,570	03/28/2001	Ryo Inoue	10559-330001 / P9842-ADI-	7113

20985 7590 08/25/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,570	INOUE ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: In claim 2, line 2, "the to" is redundant and should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Arora (U.S. Patent No. 6,442,678), hereafter referred to as Arora'678.

Referring to claims 1 and 7, Arora'678 discloses as claimed a method comprising: introducing a multi-cycle instruction (since the Arora'678'processor comprising pipelines for multi-cycle instruction, see Fig. 1, see also col. 3, lines 7-8, regarding "any pipeline stage may take any number of clock cycles") including two or more sub-instructions into a pipeline (certainly existing in the Arora'678's pipeline processor see Fig. 1); writing a result (see Col. 4, lines 50-51, indicating by the time the results data is held in latches 133 and 135, the data is also stored in SRF 106) generated in response to a sub-instruction in a speculative commit register (SRF 106, or a combination of latches 131, 133 and 136, see Fig. 1, see also Col. 1, lines 29-31, regarding the processor has finished executing an instruction and has ensured that all prior instructions will also complete, the instruction is "retired"); and writing a value in the speculative commit register (SRF 106, or a combination of latches 131, 133 and 136, see Fig. 1) to an architectural register (ARF 105, see Fig. 1) in response to the multi-cycle instruction committing (see Col. 1, lines 31-33, regarding when the instruction is "retired", the result of the

instruction may be stored in an architectural file (i.e. committed to an architectural state). Regarding claim 7, Arora'678 also discloses a machine-readable medium (such as Arora'678's main memory) which stores machine-executable instructions.

Referring to claims 13 and 22, Arora'678 discloses as claimed a processor (see Fig. 1) comprising: a pipeline operative to execute a multi-cycle instruction (since the Arora'678'processor comprising pipelines for multi-cycle instruction, see Fig. 1, see also col. 3, lines 7-8, regarding "any pipeline stage may take any number of clock cycles") including a terminal sub-instruction and a nonterminal sub-instruction (see Col. 1, lines 29-31, regarding "the processor has finished executing an instruction and has ensured that all prior instructions will also complete, the instruction is retired", note the last instruction is reasonably and broadly interpreted as a terminal sub-instruction. In addition, an instruction is also decoded and comprises several microinstructions (or sub-instructions)); an architectural register (ARF 105, see Fig. 1); a speculative commit register (SRF 106, or a combination of latches 131, 133 and 136, see Fig. 1, see also Col. 1, lines 29-31, regarding the processor has finished executing an instruction and has ensured that all prior

instructions will also complete, the instruction is "retired") operative to store results generated in responsive to the sub-instructions; and a controller (the control logic 108, see Fig. 1, or certainly existing in the Arora'678's processor such as control unit or other control logic, see also col. 4, line 66-67, and col. 5, lines 1-2, regarding the speculative results become architectural results and are stored in ARF 105) operative to control writing a result from the speculative commit register to the architectural register in response to the terminal sub-instruction committing (see Col. 1, lines 31-33, regarding when the instruction is "retired", the result of the instruction may be stored in an architectural file (i.e. committed to an architectural state). Further, regarding claim 22, Arora'678 also discloses: a system comprising: static random address memory (certainly existing in the Arora'678's system such as a cache memory see Fig. 1); and processor (certainly existing in the Arora'678's system such as a CPU see Fig. 1) coupled to the static random access memory.

As to claims 2, 8, and 16, Arora'678 also discloses: writing the value to a pointer register (see Col. 3, lines 34-39, regarding ARF 405 can be any type of register file or register stack, which inherently, stores pointer values).

As to claims 3 and 9, Arora'678 also discloses: introducing a conterminal sub-instruction and a terminal sub-instruction into the pipeline (see Col. 1, lines 29-31, regarding "the processor has finished executing an instruction and has ensured that all prior instructions will also complete, the instruction is retired", note the last instruction is reasonably and broadly interpreted as a terminal sub-instruction. In addition, an instruction is also decoded and comprises several microinstructions (or sub-instructions)).

As to claims 4 and 10, Arora'678 also discloses: writing the value in response to the terminal sub-instruction committing (as set forth above, see Col. 1, lines 31-33, regarding when the instruction is "retired", the result of the instruction may be stored in an architectural file (i.e. committed to an architectural state).

As to claims 5, 11, 18, and 23, Arora'678 also discloses: writing a stack pointer value (see Col. 3, lines 34-39, regarding ARF 405 can be any type of register file or register stack, which inherently storing stack pointer values).

As to claims 6, 12, 17, and 24, Arora'678 also discloses: writing a frame pointer value (see Col. 3, lines 34-39, regarding ARF 405 can be any type of register file or register stack, which inherently stores frame pointer values).

As to claim 14, Arora'678 also discloses: a switching element (multiplexed 109, see Fig. 1) comprising: first input data line (the output line of Merge Logic 107, see Fig. 1 since Merge Logic 107 is coupled to pipeline) coupled to the pipeline; second input data line (the feedback data line from SRF 106, see Fig. 1) coupled to the speculative commit register; and an output data line coupled to the architectural register (the output line of ARF 105, see Fig. 1), said switching element being operative to switch between the first input data line and the second input data line in response to control signals from the controller (the control logic 108, see Fig. 1).

As to claim 15, Arora'678 also discloses: the switching element comprises a multiplexed (multiplexed 109, see Fig. 1).

As to claim 19, Arora'678 also discloses: an instruction operative to invoke a subroutine (inherently existing in the Arora'678's instructions since a subroutine is either used in a program or microcode in the Arora'678's processor).

As to claim 20, Arora'678 also discloses: an instruction operative to exit a subroutine (inherently existing in the Arora'678's instructions since a subroutine is either used in a program or microcode in the Arora'678's processor).

As to claim 21, Arora'678 also discloses: an instruction operative to push or pop two or more values from a stack in

sequence (see Col. 3, lines 34-39, regarding ARF 405 can be any type of register file or register stack, which inherently, having the instruction operative to push or pop two or more values as clamed).

Response to Arguments

4. Applicant's arguments filed 6/18/04 have been fully considered but they are not deemed to be persuasive.

Applicant's response has not completely overcome claim objections.

Applicants argue that Arora fails to teach the feature of "writing a value in the speculative commit register to an architectural register in response to the multi-cycle instruction committing," as recited in Claim 1 (page 2, lines 11-14). Examiner disagrees with Applicants. As set forth above in the art rejections, Arora'678 discloses: writing a result (see Col. 4, lines 50-51, indicating by the time the results data is held in latches 133 and 135, the data is also stored in SRF 106) generated in response to a sub-instruction in a speculative commit register (SRF 106, or a combination of latches 131, 133 and 136, see Fig. 1, see also Col. 1, lines 29-31, regarding the processor has finished executing an

instruction and has ensured that all prior instructions will also complete, the instruction is "retired"); and writing a value in the speculative commit register (SRF 106, or a combination of latches 131, 133 and 136, see Fig. 1) to an architectural register (ARF 105, see Fig. 1) in response to the multi-cycle instruction committing (see Col. 1, lines 31-33, regarding when the instruction is "retired", the result of the instruction may be stored in an architectural file (i.e. committed to an architectural state). Regarding claim 7, Arora'678 also discloses a machine-readable medium (such as Arora'678's main memory) which stores machine-executable instructions.

Applicants also argue that Arora also fails to teach the feature of a multi-cycle instruction (MCI) (page 3, lines 23-24). Examiner disagrees with Applicants. As set forth above in the art rejections, Arora'678 discloses as claimed a method comprising: introducing a multi-cycle instruction (since the Arora'678'processor comprising pipelines for multi-cycle instruction, see Fig. 1, see also col. 3, lines 7-8, regarding "any pipeline stage may take any number of clock cycles") including two or more sub-instructions into a pipeline (certainly existing in the Arora'678's pipeline processor see Fig. 1).

Applicants further argue that because Arora fails to show a data flow as described in Claim 1, Arora cannot show a controller operative for such a data flow. Therefore, Arora fails to anticipate each and every feature of claims 13 and 22 (page 5, lines 5-8). Examiner disagrees with Applicants. As set forth above in the art rejections, referring to claims 13 and 22, Arora'678 discloses as claimed a processor (see Fig. 1) comprising: a pipeline operative to execute a multi-cycle instruction (since the Arora'678'processor comprising pipelines for multi-cycle instruction, see Fig. 1, see also col. 3, lines 7-8, regarding "any pipeline stage may take any number of clock cycles") including a terminal sub-instruction and a nonterminal sub-instruction (see Col. 1, lines 29-31, regarding "the processor has finished executing an instruction and has ensured that all prior instructions will also complete, the instruction is retired", note the last instruction is reasonably and broadly interpreted as a terminal sub-instruction. In addition, an instruction is also decoded and comprises several microinstructions (or sub-instructions)); an architectural register (ARF 105, see Fig. 1); a speculative commit register (SRF 106, or a combination of latches 131, 133 and 136, see Fig. 1, see also Col. 1, lines 29-31, regarding the processor has finished executing an instruction and has ensured that all prior

instructions will also complete, the instruction is "retired") operative to store results generated in responsive to the sub-instructions; and a controller (the control logic 108, see Fig. 1, or certainly existing in the Arora'678's processor such as control unit or other control logic, see also col. 4, line 66-67, and col. 5, lines 1-2, regarding the speculative results become architectural results and are stored in ARF 105) operative to control writing a result from the speculative commit register to the architectural register in response to the terminal sub-instruction committing (see Col. 1, lines 31-33, regarding when the instruction is "retired", the result of the instruction may be stored in an architectural file (i.e. committed to an architectural state). Further, regarding claim 22, Arora'678 also discloses: a system comprising: static random address memory (certainly existing in the Arora'678's system such as a cache memory see Fig. 1); and processor (certainly existing in the Arora'678's system such as a CPU see Fig. 1) coupled to the static random access memory.

Regarding Applicant's arguments about claims 2-6, 8-12, 14-21, and 23-24, Arora'678's teaching is clearly described in the art rejections as set forth above.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703)

305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

7. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
August 19, 2004